Poster

A Novel FPGA/CPU KID Readout

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A novel algorithm for performing readouts of kinetic inductance detector (KID) arrays is presented. KID arrays are valuable for their high multiplexing factor and low cost, making them ideal choices for the O(10^5) pixel instruments being proposed for the Cerro Chajnantor Atacama Telescope (CCAT). Signals are digitized and processed using an open-source field programmable gate array (FPGA) development board. The design uses a polyphase-filterbank frontend for coarse channelization, a DDC-filterbank for data-rate reduction and a linear algebra back-solve for interference rejection. In doing this, the readout problem is segregated into two sections – one of which is well-suited for the FPGA, the other for the CPU. The system has been tested in-lab and is expected to be fielded at a telescope in the near future. That revision is capable of reading 4k tones, for a system cost of $6k ($3.00/pixel for a 2-kPixel array), while consuming 40 W (~20 mW per detector). Production-scale solutions, costing $0.50/pixel (all-commercial) and <0.20/pixel (custom board) are being planned. Those solutions will use O(4mW) per pixel. Algorithms, implementation and demonstrated results will be covered.